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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, VAN THU T	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 08/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,843	FASOLI ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/21/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-17,34,36-40 and 42-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *34,36-40 and 42-49* is/are allowed.

6)☒ Claim(s) *1,3-6,8-17 and 50-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Acknowledgment is made for Amendment filed on 06/21/2006

2. Claims 1, 3-6, 8-17, 34, 36-40, 42-55 are pending.

3. Claims 2, 7, 18-33, 35, and 41 are cancelled.

4. Claims 50-55 are newly added.

Claim Rejections - 35 USC § 112

5. Claims 52-55 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 52, do Applicants mean to say one group of NAND strings coupled to its respective global bit lines at one end, and other adjacent group of NAND strings coupled to its respective global bit lines at other end? If so, it is not consistent with limitations in claim 1.

In claim 54, it is also not clear what Applicants mean. It looks like claim 54 claims for a given memory block having two or more memory planes. If so, it is also conflicted with limitation "a given memory block of a given memory plane" in claim 1 lines 5-6, which implies that a given block is on one memory plane.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3-6, 8, 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S Patent 6,118,696 (Choi) in view of U.S. Patent No. 7,012,835 (Gonzalez).

Regarding claim 1, Gonzalez discloses a memory array having at least two planes of memory cells formed above a substrate (PLANE 0 to PLANE 3, see column 8 lines 55-67 and FIG. 5), each memory plane comprising a plurality of memory blocks (e.g. BLOCK 0 - BLOCK 1, see FIG. 5), each memory block comprising a plurality floating gate memory cells being arranged in a plurality of series-connected NAND strings, each NAND string including a series selected device at each end thereof (see FIG. 7).

However, Gonzalez does not disclose how the NAND strings in a given memory block being connected to global bit lines as claimed in claim 1, lines 5-8.

Choi discloses, in FIG. 4, a memory block comprising of a plurality of floating gate memory cells being arranged in a plurality of series-connected NAND strings, said NAND strings including a series select device at each end thereof (e.g. ST1 and ST2 for first NAND string on the left), wherein each respective NAND string within the memory block is coupled to a respective global bit line that is not shared by other NAND strings within the memory block, and wherein some adjacent NAND strings of the memory block are coupled at opposite ends thereof to their respective global bit lines (see column 8, line 51 to column 9, line 45).

Since Gonzalez and Choi are both from the same field of endeavor, the purpose disclosed by Choi would have been recognized in the pertinent art of Gonzalez.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the NAND type memory cell structure disclosed in Choi for the purpose of preventing a program disturbance phenomenon from occurring in memory cells

coupled to unselected bit lines during a programming operation (see column 4, lines 51-55 and column 9, lines 63-65).

Regarding claims 3-4, Gonzalez also discloses the memory including an oxide-nitride-oxide dielectric stack (see column 1, line 66 to column 2, line 14).

Regarding claim 5, both Gonzalez and Choi do mention that the memory cells are floating gate memory cells.

Regarding claims 6 and 8, see FIG. 4 of Choi for the arrangement between NAND strings and global bit lines.

Regarding claims 50 and 52, see FIG. 4 of Choi for even and odd group B/L connected to even and odd NAND strings.

Regarding claim 51, Choi shows, in FIG. 2, a cross sectional structure of cell array having only even global bit lines 90 and 92 on the same layer, but the odd global bit lines are not in view. Therefore, it can be concluded that the even and odd global bit lines are disposed on two different layers, and that the pitch between global bit lines 90 and 92 are approximately twice the pitch of said NAND strings.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 9, 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Choi further in view of U.S. Patent No. 6,411,548 (Sakui).

Gonzalez and Choi disclose, as applied in prior rejection of claim 1, all claimed subject matter except further limitation as in claim 9.

Regarding claim 9, Sakui shows, in FIG. 74, the memory cells M0-M15 and series selection devices S1 and S2 of the NAND string 45 are structurally substantially identical.

Since Gonzalez, Choi and Sakui are all from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Gonzalez and Choi.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to have identical structure for all memory cells and the series selection device in order to simplifying and reducing the cost during manufacturing.

Regarding claims 14-17, see entire disclosure in Sakui (e.g. select gate transistors S1(s) having block insulating films 40SSL between the control [floating] gate 27SSL and charge storing layer 26SSL, see FIG. 44, etc.).

10. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Choi further in view of U.S. Patent No. 5,621,684 (Jung) or U.S. Patent No. 6,373,095 (Bracchitta) or U.S. Patent No. 6,301,155 (Fujiwara) or U.S. Patent No. 5,568,421 (Aritome).

Regarding claim 10, Jung discloses, in FIGS. 3-4, a NAND string memory array fabricated on a monocrystalline substrate (see column 6, lines 22-25).

Regarding claim 11, Bracchita discloses, in FIG. 1, a floating gate memory is formed on a polysilicon substrate (column 3, lines 17-29).

Regarding claim 12, Fujiwara discloses, in FIG. 12, a floating gate memory is formed on an SOI substrate (see column 14, lines 61-62).

Regarding claim 13, Aritome discloses, in FIG. 3, a NAND string floating gate memory cells comprising amorphous, polycrystalline silicon film, which obviously have nanoparticles (see column 5, lines 12-13).

Since Gonzalez, Choi and Jung/Bracchita/Fujiwara/Aritome are all from the same field of endeavor, the purpose disclosed by Jung/Bracchita/Fujiwara/Aritome would have been recognized in the pertinent art of Gonzalez and Choi.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to implement materials such as monocrystalline/polysilicon/SIO/Aritome for substrate or other layers because they are commercially available and commonly used in semiconductor fabrication.

Allowable Subject Matter

11. Claims 34, 36-40, 42-49 are allowed.

12. The following is an examiner's statement of reasons for allowance:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. U.S. Patent No. 6,845,030 to Kang et al., and U.S. Patent No. 6,982,902 to Gogl et al., taken individually or in combination, do not teach the claimed invention having the following limitations, in combination with the remaining claimed limitations:

As in claim 34: a memory array having a plurality of series-connected NAND strings, said memory array further comprising a second plurality of zias, each of said second plurality of zias respectively coupling to a second end of a respective NAND strings on each of two or more memory planes to an associated bias node.

FIG. 4 of Gogl et al. show a three-dimensional memory array having two memory layers, both memory layers are connected to a common global bit line 222_K via transistor 206_S or 206_{S+1}. However, Gogl et al. do not disclose those memory layers are connected to common bias node. Neither does Kang et al.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent No. 6,157,056 to Takeuchi et al, which anticipates claim 1 as shown in FIG. 19.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Thursday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

July 30, 2006

VanThu Nguyen
Primary Examiner
Art Unit 2824